Shaurya Shubham

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EXPERIENCE

Something Media — Remote
Backend Developer Intern — *Sep 2026 - Present*
- Working on a new state-of-the-art media-oriented content management system

EDUCATION

University of Wisconsin-Madison — Madison, WI
Bachelor of Science in Computer Engineering — *Sep 2023 - May 2027*
- Cumulative GPA: 3.47/4.00
- Relevant coursework: Communication Networks (ECE 537), Digital System Design & Synthesis (ECE 551), Microprocessors (ECE 353), Computer Architecture (ECE 552), Principles of IC-CAD (ECE 556), Electronic Circuits (ECE 340)

PROJECTS

PowerPC 64-bit CPU
- Designing a 64-bit PowerPC-architecture CPU in Veryl HDL, with classic 5-stage pipeline
- Randomly generated valid assembly for extensive verification
- Created a software golden model for lockstep verification with RTL

Global Routing Project
- Implemented a global routing project to route netlist pin-pairs on a grid-graph
- Used the A* algorithm to avoid physical-layer capacity overflow
- Led to a 3.5x performance improvement compared to a previous version of the project

RISC-V Processor Design
- Created a 5-stage pipelined RISC-V processor design using Verilog
- Implemented improved branch prediction using a Branch History Table and a 4-way set-associative cache

Knight's Tour Robot
- Controlled a robot to cover every square on a 5x5 chessboard using only knight moves using SystemVerilog
- Interfaced with gyroscope using SPI and communicated via UART and Bluetooth to a phone app for control
- Synthesized logic into Synopsys's cell library and successfully did post-synthesis testing

Battleship Game
- Created a two-player battleship game on the PSoC6 microprocessor platform in C with FreeRTOS
- Utilized IO from a variety of peripheral devices such as IMU sensor, light sensor, LCD, LEDs, joystick, and buttons using protocols like UART, SPI and I2C
- Implemented according to a spec and successfully interoperated with another spec-following implementation

SKILLS

Programming Languages C, C++, Rust, Java, Python, JavaScript, MATLAB

Hardware Description Languages SystemVerilog, Verilog

Technical skills SQL, Qt, Linux, Git, Mercurial(hg), FreeRTOS, Synopsys Design Compiler, ModelSim/QuestaSim